AMENDMENT TO THE CLAIMS

1. (Currently amended) A semiconductor integrated circuit system having a plurality of chips and making said plurality of chips transmit and receive signals to and from each other, comprising:

a bus selector device connected to said plurality of chips via a plurality of buses,

said bus selector device receiving connection information among said plurality of chips and selecting among connections of said plurality of buses in accordance with the connection information, and said bus selector device being provided with a first latch circuit [[means]] for holding signals to be transmitted to or received from said plurality of chips to adjust timings of signal transmission and reception,

wherein said bus selector device is further provided with a second latch circuit in which a switch signal is held, said bus selector device outputs the switch signal in accordance with the connection information among the plurality of chips and selects among connections of the plurality of buses in accordance with the switch signal.

2. (Currently amended) The semiconductor integrated circuit system of claim 1, wherein said bus selector device comprises:

switch means for switching among the connections of said plurality of buses in accordance with the switch signal; and

determination means for determining the connection information among said plurality of chips received, and for outputting [[a]] the switch signal in accordance with determination results to said switch means.

3. (Canceled)

4. (Original) The semiconductor integrated circuit system of claim 1, wherein said plurality of chips include at least one master chip and a plurality of slave chips.

5. (Original) The semiconductor integrated circuit system of claim 4, wherein

said master chip outputs the connection information among said plurality of chips to said bus selector device; and

said master chip and said bus selector device are connected to each other with a single bus, said single bus carrying the connection information among said plurality of chips.

6. (Original) The semiconductor integrated circuit system of claim 4, wherein

said master chip outputs the connection information among said plurality of chips to said bus selector device; and

said master chip and said bus selector device are connected to each other with two or more buses, one of said two or more buses carrying the connection information among said plurality of chips.

7. (Original) The semiconductor integrated circuit system of claim 6, wherein

said two or more buses include a command bus, said command bus being also used as a connection information bus to carry the connection information among said plurality of chips.

8. (Original) The semiconductor integrated circuit system of claim 6, wherein

said one of said two or more buses to carry the connection information among said plurality of chips is a specifically designed connection information bus.

9. (Original) The semiconductor integrated circuit system of claim 1, wherein the connection information among said plurality of chips is composed of a packet.

10-12. (Canceled)

13. (Currently Amended) A bus selector device connected to a plurality of chips with a plurality of buses and selecting among connections of said plurality of buses, comprising:

switch means for switching among said connections of said plurality of buses in accordance with a switch signal;

determination means for receiving and determining connection information among said plurality of chips, and for outputting [[a]] the switch signal in accordance with determination results to said switch means;

data input means for receiving data from any one of said plurality of chips;

data output means for outputting said data to at least one of said plurality of chips via one of said plurality of buses that is selected by switching of said switch means;

internal buses connected to said plurality of buses; and

a plurality of latch [[means]] circuits arranged on said plurality of internal buses, at least one of said plurality of latch circuits holds the switch signal.

14. (Original) The bus selector device of claim 13 further comprising:

control signal input means for receiving a control signal from one of said plurality of chips for another chip; and

control signal output means for outputting said control signal to at least one of said plurality of chips through one of said plurality of buses selected by switching of said switch means.

15-16. (Canceled)